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L1: Entry 4 of 8 File: DWPI Jan 12, 2001

DERWENT-ACC-NO: 2001-229262
DERWENT-WEEK: 200124

TITLE: Dry etching procedure for tungsten group laminate involves applying mixed gas containing bromine or iodine with oxygen onto polysilicon layer to form polysilicon pattern using electroconductive film as mask

PRIORITY-DATA: 1999JP-0174097 (June 21, 1999)

Takashi

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2001007085 A	January 12, 2001		009	H01L021/3065

INT-CL (IPC): H01 L 21/3065

ABSTRACTED-PUB-NO: JP2001007085A
BASIC-ABSTRACT:

NOVELTY - Tungsten group electroconductive film is etched using gas having Cl and O2 so that film thickness is higher than gap between resist films (18a,18b). Tungsten film between resist films is removed by applying gas containing I, Cl, O using films (18a,18b) as mask. Polysilicon patterns are formed by dry etching of polysilicon layer (14) selectively using gas with Br/I and O2 using conductive film as mask.

USE - Dry etching of tungsten group laminate during wiring formation.

ADVANTAGE - Improves manufacturing yield by minimizing the damage of film during etching.

DESCRIPTION OF DRAWING(S) - The figure shows section of substrate under etching process.

Polysilicon layer 14

Resist films 18a,18b

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PATENT ABSTRACTS OF JAPAN

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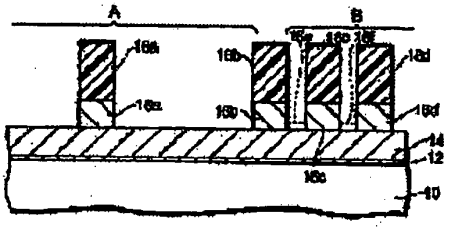
(21)Application number : 11-174097
(22)Date of filing : 21.06.1999

(71)Applicant : YAMAHA CORP
(72)Inventor : TAWARA TAKASHI

(54) DRY ETCHING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To ensure anistropic shape and lessen etching damages in laminating W-based conductive layers (W, WSi2, etc.), on a poly-Si layer.
SOLUTION: After laminating a poly-Si layer 14 and a WSi2 layer on an insulation film 12, resist layers 18a, 18b are formed on the WSi2 layer with a large gap, and resist layers 18b-18d are formed thereon with small gaps. After etching the WSi2 layer with a plasma of Cl2/O2 gas, by having it overetched to remove WSi2 layers 16e, 16f with a plasma of HBr/Cl2/O2 gas while reaction products suppress side etching, WSi2 layers 16a-16d corresponding to the layers 18a-18d are thereby obtained. The layer 14 is selectively etched with a plasma of HBr/Cl2/O2 gas, while reaction products suppress side etching. The method is also applicable to single layers of W-based conductive materials.



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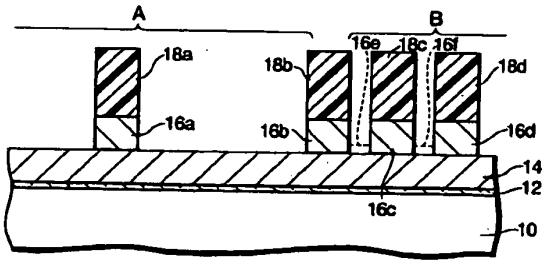
BB18 CA01 DA00 DA02 DA04
DA18 DA25 DA26 DB02 DB10
DB17 EA28 EB02

(54)【発明の名称】　ドライエッチング方法

(57)【要約】
【課題】　Ｗ系導電材層（Ｗ，ＷＳｉ₂等）をポリＳｉ層に重ねた積層のドライエッチング方法において、異方性形状の確保とエッチングダメージの軽減とを可能にする。
【解決手段】　絶縁膜１２の上にポリＳｉ層１４及びＷＳｉ₂層の積層を形成した後、ＷＳｉ₂層の上にレジスト層１８ａ，１８ｂを大間隔で、レジスト層１８ｂ～１８ｄを小間隔でそれぞれ形成する。Ｃｌ₂／Ｏ₂ガスのプラズマでＷＳｉ₂層をジャストエッチングした後、ＨＢｒ／Ｃｌ₂／Ｏ₂ガスのプラズマにより反応生成物でサイドエッチングを抑制しつつオーバーエッチングを行なってＷＳｉ₂層１６ｅ，１６ｆを除去することにより層１８ａ～１８ｄに対応するＷＳｉ₂層１６ａ～１６ｄを得る。ＨＢｒ／Ｃｌ₂／Ｏ₂ガスのプラズマにより反応生成物でサイドエッチングを抑制しつつ層１４を選択的にエッチングする。本方法は、Ｗ系導電材の単層にも応用できる。



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【特許請求の範囲】

【請求項1】基板を覆う絶縁膜の上に、ポリシリコン層にタングステン系導電材層を重ねた積層を形成する工程と、

前記タングステン系導電材層の上に複数のレジスト層を互いに接近させて形成する工程と、

塩素含有ガス及び酸素ガスの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより前記タングステン系導電材層をその厚さが前記複数のレジスト層の間の間隔より広いレジスト不存在領域にてゼロ又はその近傍の値になるようにエッチングする工程と、

臭素含有ガスはヨウ素含有ガスと塩素含有ガスと酸素ガスとの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより反応生成物で前記タングステン系導電材層のサイドエッチングを抑制しつつ前記複数のレジスト層の間のタングステン系導電材を除去することにより前記複数のレジスト層にそれぞれ対応したパターンを有する複数のタングステン系導電材層を形成する工程と、

少なくとも臭素含有ガス又はヨウ素含有ガスと酸素ガスとを含む混合ガスをエッチングガスとし且つ前記複数のレジスト層及び前記複数のタングステン系導電材層をマスクとするドライエッチングにより前記ポリシリコン層を選択的に除去することにより前記複数のレジスト層にそれぞれ対応したパターンを有する複数のポリシリコン層を形成する工程とを含むドライエッチング方法。

【請求項2】基板を覆う絶縁膜の上にタングステン系導電材層を形成する工程と、

前記タングステン系導電材層の上に複数のレジスト層を互いに接近させて形成する工程と、

塩素含有ガス及び酸素ガスの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより前記タングステン系導電材層をその厚さが前記複数のレジスト層の間の間隔より広いレジスト不存在領域にてゼロ又はその近傍の値になるようにエッチングする工程と、

臭素含有ガス又はヨウ素含有ガスと塩素含有ガスと酸素ガスとの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより反応生成物で前記タングステン系導電材層のサイドエッチングを抑制しつつ前記複数のレジスト層の間のタングステン系導電材を除去することにより前記複数のレジスト層にそれぞれ対応したパターンを有する複数のタングステン系導電材層を形成する工程とを含むドライエッチング方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】この発明は、W（タングステン）、WSi_2（タングステンシリサイド）等のW系導電材層をポリSi（シリコン）層に重ねた積層又はW系導電材の単層をドライエッチングする方法に関し、特にCl（塩素）含有ガスとO_2（酸素）ガスとの混合ガスをエッチングガスとするドライエッチングによりW系導電材層をジャストエッチングした後該混合ガスにBr（臭素）含有ガス又はI（ヨウ素）含有ガスを添加してオーバーエッチングを行なうことにより異方性形状の確保とエッチングダメージの軽減とを可能にしたものである。

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【0002】

【従来の技術】従来、WSi_2層をポリSi層に重ねた積層（Wポリサイド層）を用いる配線形成法としては、図11～13に示すような方法が知られている（例えば、特開平7－94469号公報参照）。

【0003】図11の工程では、シリコン基板1の表面を覆うゲート酸化膜2の上にポリSi層3及びWSi_2層4を順次に堆積形成した後、WSi_2層4の上にホトリソグラフィ処理によりレジスト層5a～5dを形成する。レジスト層5a，5bは、疎パターン領域aにおいて大きな間隔で配置し、レジスト層5b～5dは、密パターン領域bにおいて小さな間隔で配置する。

【0004】図12の工程では、F（フッ素）含有ガス（例えばS_2F_6ガス）を用いるプラズマエッチングによりポリSi層3及びWSi_2層4の積層を疎パターン領域aにて厚さがゼロ又はその近傍の値になるようにジャストエッチングする。この結果、レジスト層5a～5dにそれぞれ対応したパターンを有するWSi_2層4a～4dが残存する。また、密パターン領域bでは、いわゆるRIElag現象（又はマイクロローディング効果）によりエッチング速度が低下するため、疎パターン領域aにおけるポリSi層3の被エッチング部3eに比べてポリSi層3の被エッチング部3fが厚く残存する。

【0005】図13の工程では、Br含有ガス（例えばHBrガス）及びO_2ガスの混合ガスを用いるプラズマエッチングによりオーバーエッチングを行なってポリSi層3における3e，3f等の被エッチング部を除去する。HBr等のBr系ガスとO_2ガスとの混合ガスを用いるプラズマエッチングは、ゲート酸化膜2に対するポリSi層3の選択性が高い。オーバーエッチングの結果として、レジスト層5a～5dにそれぞれ対応したパターンを有するポリSi層3a～3dが残存する。オーバーエッチング時には、パターン側壁に付着した反応生成物がWSi_2層4a～4d及びポリSi層3a～3dのサイドエッチングを抑制するので、4a／3a，4b／3b，4c／3c，4d／3d等の積層に異方性形状を持たせることができる。オーバーエッチングの後は、レジスト層5a～5dを除去する。4a／3a等の積層は、ゲート電極乃至配線層として使用される。

【0006】従来、W層を用いる配線形成法としては、

図１４～１６に示すような方法が提案されている。

【０００７】図１４の工程では、シリコン等の半導体基板６の表面を覆うシリコンオキサイド等の絶縁膜７の上にＷ層８を形成する。そして、Ｗ層８の上にレジスト層９ａ，９ｂを互いに接近させて形成する。

【０００８】図１５の工程では、Ｆ含有ガスとしてＳＦ６を用いるプラズマエッチングによりＷ層８をレジスト層９ａ，９ｂ間の間隔より広いレジスト不存在領域にて厚さがゼロ又はその近傍の値になるようにジャストエッチングする。この結果、レジスト層９ａ，９ｂにそれぞれ対応したＷ層８ａ，８ｂが残存すると共に、Ｗ層８ａ，８ｂの間にはＲＩＥｌａｇ現象により薄いＷ層８ｃが残存する。

【０００９】図１６の工程では、図１５の工程に引き続いて図１５の工程と同様のプラズマエッチングによりオーバーエッチングを行なってＷ層８ｃを除去し、Ｗ層８ａ，８ｂを残存させる。この後、レジスト層９ａ，９ｂを除去する。Ｗ層８ａ，８ｂは、配線層として使用される。

【００１０】図１５，１６のＳＦ６によるプラズマエッチング工程において、異方性エッチングを行なうには、基板に入射するイオンのエネルギーを高くしたり、基板の温度を低くしたりする必要がある。また、反応生成物でサイドエッチングを抑制して異方性形状を確保する方法も提案されている。例えば、特開平７－１４７２７１号公報には、ＳＦ６にＮ２やＮＨ３を添加したガスのプラズマでＷ層をエッチングすることにより反応生成物であるＷＮによりサイドエッチングを抑制することが示されている。特開平１０－３２６７７４号公報にも、ＳＦ６にＣＨＦ３及びＮ２を添加したガスのプラズマでＷ層をエッチングする方法が示されている。特開平７－１６９７４４号公報には、Ｗ層の下にＴｉ又はＴｉ化合物の膜を敷き、エッチング活性種であるＦとＴｉとの反応で生成される低蒸気圧のフッ化チタンでサイドエッチングを抑制することが示されている。

【００１１】

【発明が解決しようとする課題】図１１～１３の方法によると、下地にエッチングダメージが生じやすい。すなわち、図１３のオーバーエッチング工程では、前述したようにゲート酸化膜２に対するポリＳｉ層３の選択比が高いものの、図１２のジャストエッチング工程では、フッ素系ガスのプラズマでエッチングを行なうので、ゲート酸化膜２に対するポリＳｉ層３の選択比が低く、ゲート酸化膜２がエッチングされることがある。これを防ぐには、ポリＳｉ層３の厚さがゼロになる前にジャストエッチングを停止するように工程管理を厳しくする必要がある。また、ゲート絶縁膜２を含むゲート部は、図１２のジャストエッチング時及び図１３のオーバーエッチング時にプラズマにさらされるので、イオン衝撃によるダメージを受けやすい。

【００１２】一方、図１４～１６の方法によると、フッ素系ガスのプラズマでエッチングを行なうので、絶縁膜７を構成するシリコンオキサイドに対するＷの選択比が低く、図１６に示すようにオーバーエッチングの際に絶縁膜７がＷ層８ａ，８ｂの側方でエッチングされる。このため、配線段差が大きくなる不都合がある。

【００１３】この発明の目的は、異方性形状を確保しつつエッチングダメージを軽減することができる新規なドライエッチング方法を提供することにある。

【００１４】

【課題を解決するための手段】この発明に係る第１のドライエッチング方法は、基板を覆う絶縁膜の上に、ポリシリコン層にタングステン系導電材層を重ねた積層を形成する工程と、前記タングステン系導電材層の上に複数のレジスト層を互いに接近させて形成する工程と、塩素含有ガス及び酸素ガスの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより前記タングステン系導電材層をその厚さが前記複数のレジスト層の間の間隔より広いレジスト不存在領域にてゼロ又はその近傍の値になるようにエッチングする工程と、少なくとも臭素含有ガス又はヨウ素含有ガスと酸素ガスとを含む混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより反応生成物で前記タングステン系導電材層のサイドエッチングを抑制しつつ前記複数のレジスト層の間のタングステン系導電材を除去することにより前記複数のレジスト層にそれぞれ対応したパターンを有する複数のタングステン系導電材層を形成する工程と、臭素含有ガス又はヨウ素含有ガスと塩素含有ガスと酸素ガスとの混合ガスをエッチングガスとし且つ前記複数のレジスト層及び前記複数のタングステン系導電材層をマスクとするドライエッチングにより前記ポリシリコン層を選択的に除去することにより前記複数のレジスト層にそれぞれ対応したパターンを有する複数のポリシリコン層を形成する工程とを含むものである。

【００１５】第１のドライエッチング方法によれば、Ｃｌ２等の塩素含有ガス及びＯ２ガスの混合ガスをエッチングガスとするドライエッチングによりＷ，ＷＳｉ２等のＷ系導電材層をジャストエッチングした後該混合ガスにＨＢｒ等の臭素含有ガス（又はヨウ素含有ガス）を添加してＷ系導電材のオーバーエッチングを行ない、この後ポリＳｉ単層のドライエッチングを行なう。オーバーエッチングでは、Ｏ２ガスの流量割合を高く設定することによりポリＳｉに対するＷ系導電材の選択比を高くすることができ、Ｗ系導電材を選択的に除去することが可能となる。また、オーバーエッチングでは、臭素含有ガス（又はヨウ素含有ガス）の流量割合を所定の値に設定することによりＷ系導電材について異方性形状を確保しつつエッチングを行なうことができる。さらに、ジャストエッチング及びオーバーエッチングは、下地膜として

の絶縁膜の上にポリSi層が存在する状態で行なわれるので、下地膜（絶縁膜）がエッチングされたり、イオン衝撃にさらされたりすることがなく、エッチングダメージの軽減が可能となる。

【0016】この発明に係る第2のエッチング方法は、基板を覆う絶縁膜の上にタングステン系導電材層を形成する工程と、前記タングステン系導電材層の上に複数のレジスト層を互いに接近させて形成する工程と、塩素含有ガス及び酸素ガスの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより前記タングステン系導電材層をその厚さが前記複数のレジスト層の間の間隔より広いレジスト不存在領域にてゼロ又はその近傍の値になるようにエッチングする工程と、臭素含有ガス又はヨウ素含有ガスと塩素含有ガスと酸素ガスとの混合ガスをエッチングガスとし且つ前記複数のレジスト層をマスクとするドライエッチングにより反応生成物で前記タングステン系導電材層のサイドエッチングを抑制しつつ前記複数のレジスト層の間のタングステン系導電材を除去することにより前記複数のレジスト層にそれぞれ対応したパターンを有する複数のタングステン系導電材層を形成する工程とを含むものである。

【0017】第2のドライエッチング方法によれば、Cl_2等の塩素含有ガス及びO_2ガスの混合ガスをエッチングガスとするドライエッチングによりW，WSi_2等のW系導電材層をジャストエッチングした後該混合ガスにHBr等の臭素含有ガス（又はヨウ素含有ガス）を添加してW系導電材のオーバーエッチングを行なう。ジャストエッチング及びオーバーエッチングのいずれにおいても、塩素含有ガス及びO_2ガスの混合ガスをエッチングガスとして用いるので、下地膜としての絶縁膜を構成するシリコンオキサイド等に対する選択比が向上し、下地膜（絶縁膜）のエッチングを抑制することができる。また、オーバーエッチングでは、臭素含有ガス（又はヨウ素含有ガス）の添加によりW系導電材のサイドエッチングが抑制されるので、良好な異方性形状を得ることができる。

【0018】

【発明の実施の形態】図1～3は、この発明の一実施形態に係る配線形成法を示すものである。

【0019】図1の工程では、シリコン等の半導体基板10の表面に熱酸化法等によりシリコンオキサイドからなるゲート絶縁膜12を形成する。ゲート絶縁膜12の上には、CVD（ケミカル・ベーパー・デポジション）法等によりポリSi層14及びWSi_2層16を順次に堆積形成する。ポリSi層14及びWSi_2層16は、ゲート電極乃至配線層を形成するためのもので、ポリSi層14は、導電型決定不純物のドーピングにより低抵抗化されている。

【0020】WSi_2層16の上には、周知のホトリソグラフィ処理により所望のゲート電極・配線パターンに従ってレジスト層18a～18dを形成する。レジスト層18a，18bは、疎パターン領域Aにおいて大きな間隔で配置し、レジスト層18b～18dは、密パターン領域Bにおいて小さな間隔で配置する。

【0021】図2の工程では、Cl_2ガス及びO_2ガスの混合ガス（Cl_2/O_2ガス）を用いるプラズマエッチングによりWSi_2層16を疎パターン領域Aにて厚さがゼロ又はその近傍の値になるようにジャストエッチングする。このときのエッチングは、一例として図4のECR（電子サイクロトロン共鳴）型プラズマエッチング装置を用いて行ない、エッチング条件は、

圧力：1mTorr

マイクロ波電力：1000W

高周波電力：50W

ガス流量：Cl_2/O_2＝50／10sccm

とした。

【0022】ジャストエッチングの結果として、レジスト層18a～18bにそれぞれ対応したパターンを有するWSi_2層16a～16dが残存する。また、密パターン領域Bでは、RIElag現象によりエッチング速度が低下するため、比較的薄いWSi_2層16e及び16fがWSi_2層16b，16cの間及びWSi_2層16c，16dの間にそれぞれ残存する。

【0023】この後、Cl_2/O_2ガスにHBrガスを添加したHBr／Cl_2/O_2ガスを用いるプラズマエッチングによりオーバーエッチングを行なってWSi_2層16e，16fを除去する。このときのエッチングは、一例として図4のエッチング装置を用いて行ない、エッチング条件は、

圧力：1mTorr

マイクロ波電力：1000W

高周波電力：50W

ガス流量：HBr／Cl_2/O_2＝8．5／21．5／20sccm

とした。

【0024】オーバーエッチングにおいてO_2流量割合を高くしたのは、ポリSiに対するWSi_2の選択比を高くして16e，16f等のWSi_2層の除去を容易にするためである。このようにO_2流量割合の高いCl_2/O_2エッチングプロセスでは、Wが蒸気圧の高い$WOCl_4$となってWSi_2層16a～16dの側壁をエッチング（サイドエッチング）し、WSi_2層16a～16dの異方性形状が損なわれる。そこで、オーバーエッチング時には、Cl_2/O_2ガスにHBrを添加して蒸気圧の低い$WOBr_4$やWBr_5を生成させてWSi_2層16a～16dの側壁に保護膜を形成しつつ（サイドエッチングを抑制しつつ）エッチングを行なう。この結果、WSi_2層16a～16dの異方性形状が確保される。また、ジャストエッチング及びオーバーエッチング

は、ゲート絶縁膜１２上にポリＳｉ層１４が存在する状態で行なわれるので、ゲート絶縁膜１２がエッチングされたり、イオン衝撃にさらされたりすることがなく、エッチングダメージが軽減される。

【００２５】図３の工程では、ＨＢｒ／Ｃｌ$_2$／Ｏ$_2$ガスを用いるプラズマエッチングによりレジスト層１８ａ～１８ｄ及びＷＳｉ$_2$層１６ａ～１６ｄをマスクとしてポリＳｉ層１４を選択的にエッチングする。このエッチングは、一例として図４のエッチング装置を用いて行ない、エッチング条件は、

圧力：２ｍＴｏｒｒ

マイクロ波電力：１０００Ｗ

高周波電力：３５Ｗ

ガス流量：ＨＢｒ／Ｃｌ$_2$／Ｏ$_2$＝１００／５／５ｓｃｃｍ

とした。エッチング条件の他の例としては、Ｃｌ$_2$等の塩素含有ガスを用いないものも可能であり、マイクロ波電力：８００～１５００Ｗ、ガス流量：ＨＢｒ／Ｏ$_2$＝１００／５ｓｃｃｍとすることができる。

【００２６】ポリＳｉ層１４の選択エッチングの結果として、レジスト層１８ａ～１８ｄにそれぞれ対応したパターンを有するポリＳｉ層１４ａ～１４ｄが残存する。ポリＳｉエッチング時には、ＳｉＯ$_x$，ＳｉＢｒ$_x$等の反応生成物がＷＳｉ$_2$層１６ａ～１６ｄ及びポリＳｉ層１４ａ～１４ｄのサイドエッチングを抑制するので、１６ａ／１４ａ，１６ｂ／１４ｂ，１６ｃ／１４ｃ，１６ｄ／１４ｄ等の積層に良好な異方性形状を持たせることができる。ポリＳｉは、ＷＳｉ$_2$に比べてＲＩＥｌａｇが少なく、エッチングしやすい。ポリＳｉエッチングの後は、周知のアッシング処理によりレジスト層１８ａ～１８ｄを除去する。１６ａ／１４ａ等のＷＳｉ$_2$／ポリＳｉ積層は、ゲート電極乃至配線層として使用される。

【００２７】発明者は、Ｃｌ$_2$／Ｏ$_2$ガスを用いるプラズマエッチングがＷＳｉ$_2$／ポリＳｉ積層（Ｗポリサイド層）のエッチングにおいてポリＳｉに対するＷＳｉ$_2$の選択比を高く設定可能である点に着目し、図４のエッチング装置を用いて種々の実験を行なった。

【００２８】図４の装置において、処理室２０は、プラズマ室２２ａ及び反応室２２ｂからなっている。反応室２２ｂの底部には、試料台（電極）２４が設けられており、試料台２４の上面には、被処理ウエハ２６が載置される。

【００２９】試料台２４には、高周波電源２８が接続され、例えば１３．５６ＭＨｚの高周波電力が供給される。反応室２２ｂは、図示しないガス供給源に接続されると共に排気装置ＶＡＣに接続される。

【００３０】プラズマ室２２ａの上部には、図示しないマイクロ波電源からマイクロ波導入窓３０を介して例えば２．４５ＧＨｚのマイクロ波ＭＷが供給される。窓３０は、通常、石英で構成される。処理室２０の上部を取

囲むようにソレノイドコイル３２が設けられている。

【００３１】図４のエッチング装置を用いてＣｌ$_2$／Ｏ$_2$ガスのプラズマでＷＳｉ$_2$及びポリＳｉのエッチングを行ない、ＷＳｉ$_2$／ポリＳｉ選択比のＯ$_2$流量割合依存性を調べた結果を図５に示す。実験には、シリコン基板上にシリコンオキサイド膜を介してＷＳｉ$_2$層を堆積形成したサンプルを９個含む第１のサンプル群と、シリコン基板上にシリコンオキサイド膜を介してポリＳｉ層を堆積形成したサンプルを９個含む第２のサンプル群とを用いた。各シリコン基板の直径は、２００ｍｍとした。各サンプルを図４のエッチング装置内に被処理ウエハ２６として挿入し、エッチングを行なった。エッチング条件は、

圧力：１ｍＴｏｒｒ

マイクロ波電力：１４００Ｗ

高周波電力：５０Ｗ

ガス流量：Ｃｌ$_2$＋Ｏ$_2$＝５０ｓｃｃｍ

とした。

【００３２】第１のサンプル群中の９個のサンプルについては、Ｏ$_2$流量割合を０，１０，２０，２２，２４，２６，２８，３０，４０％のように変化させ、各サンプル毎にＷＳｉ$_2$のエッチング速度を求めた。その結果を図５にて線Ｐで示す。また、第２のサンプル群中の９個のサンプルについては、Ｏ$_2$流量割合を第１のサンプル群の場合と同様に変化させ、各サンプル毎にポリＳｉのエッチング速度を求めた。その結果を図５にて線Ｑで示す。

【００３３】ＷＳｉ$_2$／ポリＳｉ選択比は、第１のサンプル群と第２のサンプル群とでＯ$_2$流量割合が同じサンプル毎にＷＳｉ$_2$のエッチング速度／ポリＳｉのエッチング速度の比を求めることにより算出した。その結果を図５にて線Ｒで示す。

【００３４】図５の実験結果によれば、Ｏ$_2$の流量割合を３０％以上にすれば、ほぼＷＳｉ$_2$のみがエッチングされるプロセス条件になることがわかる。図２のオーバーエッチングでは、Ｏ$_2$の流量割合を４０％としたので、狭いスペースに残存した１６ｅ，１６ｆ等のＷＳｉ$_2$層を効率的に除去することができる。その結果、ＷＳｉ$_2$のＲＩＥｌａｇ現象に基づくエッチング速度のパターン依存性をキャンセルすることができる。

【００３５】図６は、ＨＢｒ／Ｃｌ$_2$／Ｏ$_2$ガスを用いるプラズマエッチングにおけるＷＳｉ$_2$サイドエッチング量のＨＢｒ流量割合依存性を調べた結果を示すものである。実験には、直径２００ｍｍのシリコン基板上にシリコンオキサイド膜を介してＷＳｉ$_2$／ポリＳｉ積層（Ｗポリサイド層）を形成したサンプルを４個用いた。各サンプルには、図１の密パターン領域Ｂに示すようにライン／スペース＝１．０／０．６μｍのパターンに従って多数のレジスト層を並設した。このようにレジスト層を設けた各サンプルを図４のエッチング装置内に被処

理ウエハ２６として挿入し、エッチングを行なった。エッチング条件は、

圧力：１ｍＴｏｒｒ

マイクロ波電力：１４００Ｗ

高周波電力：５０Ｗ

ガス流量：Cl_2＋ＨＢｒ＝３０ｓｃｃｍ，O_2＝２０ｓｃｃｍ

とした。ここで、O_2流量割合は、図１でＷSi_2／ポリＳｉ選択比が無限大となる４０％である。

【００３６】４個のサンプルについては、Cl_2＋ＨＢｒのうちＨＢｒを０，１０，２０，３０％のように変化させ、各サンプル毎にＷSi_2のサイドエッチング量Ｓ（μｍ）を求めた。サイドエッチング量Ｓは、図７にＷSi_2層１６ａに関して例示するようにＳ＝頂面で測定した幅Ｗｔｏｐ－底面で測定した幅Ｗｂｏｔとして求めることができる。Ｓ＜０は順テーパ形状を、Ｓ＞０はサイドエッチ形状（逆テーパ形状）をそれぞれ表わす。

【００３７】図６の実験結果によれば、ＨＢｒ流量割合１７％でサイドエッチングがゼロとなり、垂直な異方性エッチング形状が得られることがわかる。しかしながら、ＨＢｒ流量割合１７％の条件にすると、ライン／スペースパターンでは垂直形状が得られるものの、孤立ラインでは側壁に多量の反応生成物が付着するため、順テーパ形状になってしまう。

【００３８】図２の工程では、Cl_2／O_2ガスを用いるプラズマエッチングでジャストエッチングを行なうようにしたので、ＨＢｒ／Cl_2／O_2プロセスで起こったような孤立ラインでの順テーパ形状の発生を防ぐことができる。また、高O_2流量のＨＢｒ／Cl_2／O_2ガスプラズマエッチングプロセスを用いてＷSi_2のオーバーエッチングを行なうようにしたので、ポリＳｉに対するＷSi_2の選択比を高く保ちながら、狭いスペースに残存したＷSi_2のみをエッチング除去することができ、しかもＨＢｒの添加効果によりＷSi_2のサイドエッチングを防ぐことができる。

【００３９】図８～１０は、この発明の他の実施形態に係る配線形成法を示すものである。

【００４０】図８の工程では、シリコン等の半導体基板４０の表面を覆うシリコンオキサイド等の絶縁膜４２の上にＷ層４４をスパッタ法等により形成する。そして、Ｗ層４４の上に所望の配線パターンに従ってレジスト層４６ａ，４６ｂを互いに接近させて形成する。

【００４１】図９の工程では、Cl_2／O_2ガスを用いるプラズマエッチングによりＷ層４４をレジスト層４６ａ，４６ｂの間隔より広いレジスト不存在領域で厚さがゼロ又はその近傍の値になるようにジャストエッチングする。このときのエッチングは、図２で述べたジャストエッチングと同様の条件で行なうことができる。ジャストエッチングの結果として、レジスト層４６ａ，４６ｂにそれぞれ対応したＷ層４４ａ，４４ｂが得られると共に、Ｗ層４４ａ，４４ｂの間にはＲＩＥｌａｇ現象により薄いＷ層４４ｃが残存する。

【００４２】図１０の工程では、Cl_2／O_2ガスにＨＢｒを添加したＨＢｒ／Cl_2／O_2ガスを用いるプラズマエッチングによりオーバーエッチングを行なってＷ層４４ｃを除去し、Ｗ層４４ａ，４４ｂを残存させる。このときのエッチングは、図２で述べたオーバーエッチングと同様の条件で行なうことができる。オーバーエッチングの後は、レジスト層４６ａ，４６ｂをアッシング処理等により除去する。Ｗ層４４ａ，４４ｂは、配線層として使用される。

【００４３】図９，１０のエッチング処理では、Cl_2／O_2ガスをエッチングガスとして用いるので、絶縁膜４２を構成するシリコンオキサイドに対するＷの選択比が向上する。従って、絶縁膜４２の膜減りや配線段差の増大を防止することができる。また、図１０のオーバーエッチングでは、ＨＢｒの添加によりＷ層４４ａ，４４ｂのサイドエッチングが抑制されるので、Ｗ層の形状劣化（逆テーパ形状等）を防ぐことができる。

【００４４】図８～１０に関して上記した配線形成法は、Ｗ層４４の代りにＷSi_2層を用いて実施してもよく、上記したと同様の作用効果が得られる。

【００４５】この発明は、上記した実施形態に限定されるものではなく、種々の改変形態で実施可能なものである。例えば、次のような変更が可能である。

【００４６】（１）Ｗ系導電材層としては、Ｗ，ＷSi_2に限らず、Ｗ合金を用いてもよい。タングステンシリサイドとしては、ＷSi_2のように化学量論的なものに限らず、非化学量論的なものを用いてもよく、一般的にはＷSi_xを使用可能である。

【００４７】（２）臭素含有ガスとしては、ＨＢｒに限らず、Br_2，BBr_3，CBr_4，$SiBr_4$等を用いてもよい。Br_2等のガスの添加量は、プラズマ中に存在するＢｒ原子の量が前記実施形態で示したＨＢｒの場合と同等になるように設定すればよい。また、臭素含有ガスの代りに、ＨＩ，I_2，BI_3，CI_4，SiI_4等のヨウ素含有ガスを用いてもよい。ＨＢｒ又はＨＩ等のガスあるいはO_2ガスについて、添加量の最適値は、被エッチング膜の膜質に依存する（例えば、成膜方法、成膜後の処理条件、成膜装置等に依存する）ので、被エッチング膜毎に調整するのが望ましい。

【００４８】（３）Ｗ系導電材層をドライエッチングする場合、Ｗ系導電材層の上に予めＴｉＮ，ＴｉＯＮ等の反射防止膜を設けておいてもよい。また、Ｗ系導電材層とポリＳｉ層との間にＷＮ層等を介在させておいてもよい。

【００４９】

【発明の効果】以上のように、この発明によれば、塩素系ガス及び酸素ガスの混合ガスをエッチングガスとするドライエッチングによりＷ系導電材層をジャストエッチ

ングした後該混合ガスに臭素含有ガス（又はヨウ素含有ガス）を添加してW系導電材のオーバーエッチングを行ない、この後ポリSi単層のドライエッチングを行なうようにしたので、異方性形状を確保しつつエッチングダメージを軽減することができ、歩留りが向上する効果が得られる。

【0050】また、塩素含有ガス及び酸素ガスの混合ガスをエッチングガスとするドライエッチングによりW系導電材層をジャストエッチングした後該混合ガスに臭素含有ガス（又はヨウ素含有ガス）を添加してW系導電材のオーバーエッチングを行なうようにしたので、異方性形状を確保しつつ下地絶縁膜のエッチングを抑制することができ、歩留りが向上する効果が得られる。

【図面の簡単な説明】

【図1】 この発明の一実施形態に係る配線形成法におけるレジスト層形成工程を示す基板断面図である。

【図2】 図1の工程に続くWSi_2層のジャストエッチング工程及びオーバーエッチング工程を示す基板断面図である。

【図3】 図2の工程に続くポリSi層エッチング工程及びレジスト層除去工程を示す基板断面図である。

【図4】 この発明の実施に用いられるプラズマエッチング装置を示す断面図である。

【図5】 Cl_2/O_2ガスを用いるプラズマエッチングにおける選択比（WSi_2／ポリSi）のO_2流量割合依存性を示すグラフである。

【図6】 HBr／Cl_2／O_2ガスを用いるプラズマ

エッチングにおけるWSi_2サイドエッチング量のHBr流量割合依存性を示すグラフである。

【図7】 WSi_2／ポリSi積層エッチングにおけるWSi_2層のサイドエッチング状況を示す断面図である。

【図8】 この発明の他の実施形態に係る配線形成法におけるレジスト層形成工程を示す基板断面図である。

【図9】 図8の工程に続くW層のジャストエッチング工程を示す基板断面図である。

【図10】 図9の工程に続くオーバーエッチング工程を示す基板断面図である。

【図11】 従来の配線形成法の一例におけるレジスト層形成工程を示す基板断面図である。

【図12】 図11の工程に続くWSi_2／ポリSi積層のジャストエッチング工程を示す基板断面図である。

【図13】 図12の工程に続くオーバーエッチング工程及びレジスト層除去工程を示す基板断面図である。

【図14】 従来の配線形成法の他の例におけるレジスト層形成工程を示す基板断面図である。

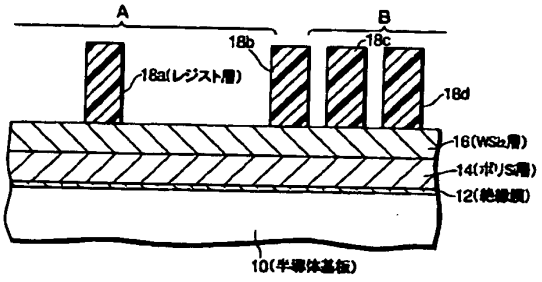
【図15】 図14の工程に続くW層のジャストエッチング工程を示す基板断面図である。

【図16】 図15の工程に続くオーバーエッチング工程を示す基板断面図である。

【符号の説明】

10，40：半導体基板、12，42：絶縁膜、14，ポリSi層，16：WSi_2層、18a～18d，46a，46b：レジスト層、44：W層。

【図1】



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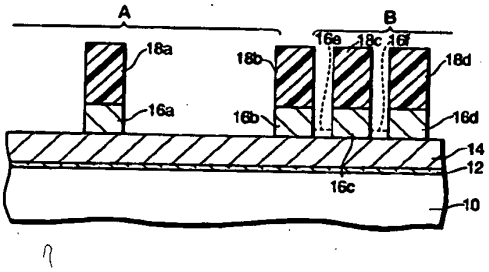

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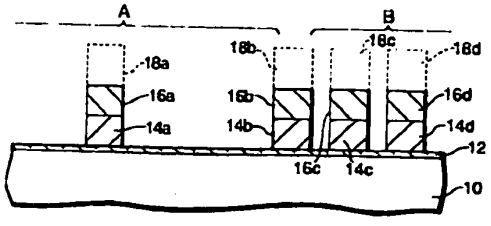

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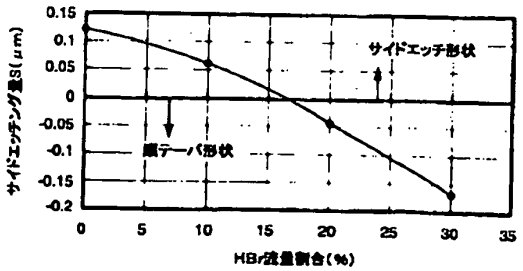

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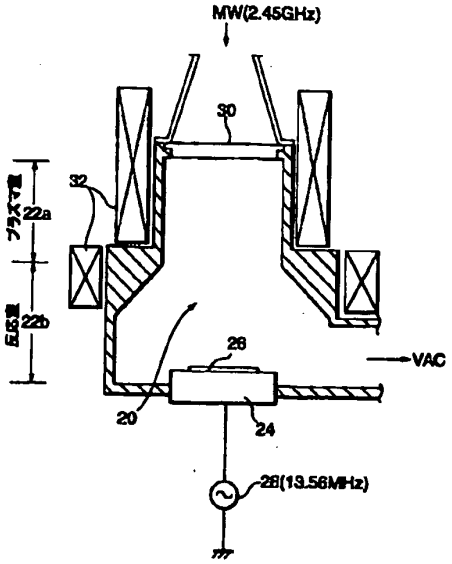

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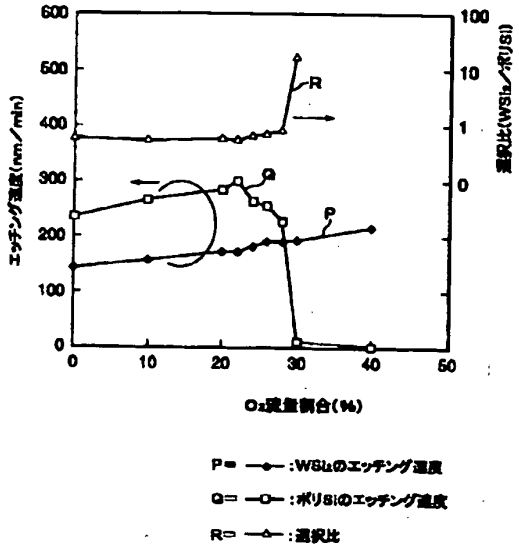

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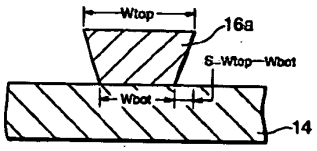

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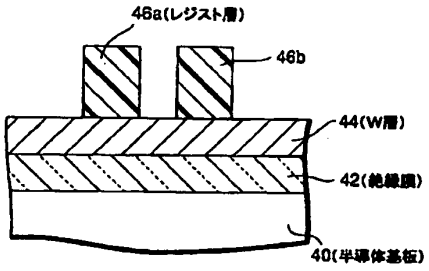

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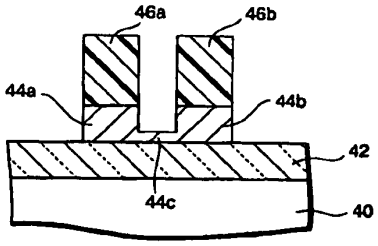

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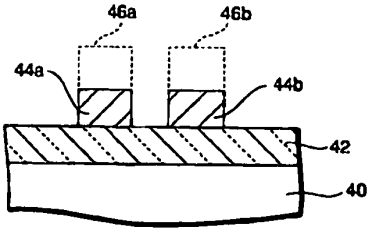

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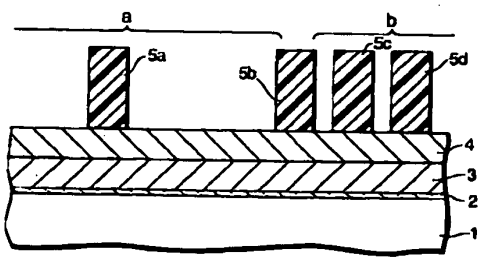

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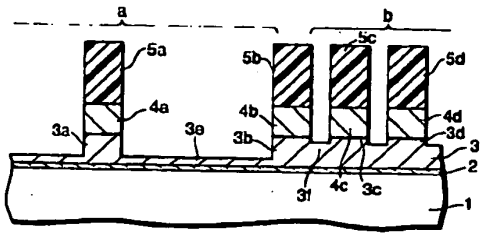

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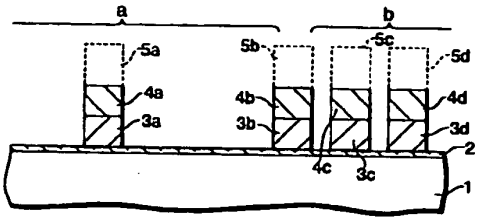

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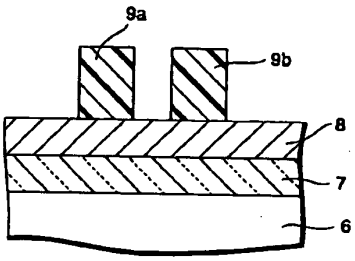

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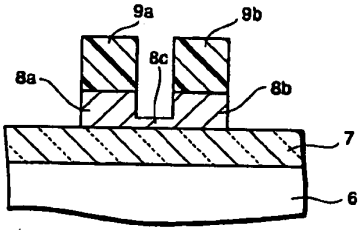

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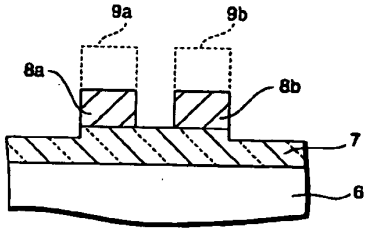

JP2001-007085

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The process which forms the laminating which put the tungsten system electric conduction material layer for the substrate on the polish recon layer on the wrap insulator layer, The process which two or more resist layers are made to approach mutually, and forms them on said tungsten system electric conduction material layer, By the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, and uses said two or more resist layers as a mask The process which etches said tungsten system electric conduction material layer so that the thickness may become the value of zero or its near in a resist non-existence region larger than spacing between said two or more resist layers, Bromine content gas by the dry etching which makes etching gas the mixed gas of iodine content gas, chlorine content gas, and oxygen gas, and uses said two or more resist layers as a mask The process which forms two or more tungsten system electric conduction material layers which have a pattern corresponding to said two or more resist layers, respectively by removing the tungsten system electric conduction material between said two or more resist layers, controlling side etching of said tungsten system electric conduction material layer with a resultant, By the dry etching which makes etching gas the mixed gas which contains bromine content gas or iodine content gas, and oxygen gas at least, and uses said two or more resist layers and said two or more tungsten system electric conduction material layers as a mask The dry etching approach including the process which forms two or more polish recon layers which have a pattern corresponding to said two or more resist layers by removing said polish recon layer alternatively, respectively.
[Claim 2] The process which forms a tungsten system electric conduction material layer for a substrate on a wrap insulator layer, The process which two or more resist layers are made to approach mutually, and forms them on said tungsten system electric conduction material layer, By the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, and uses said two or more resist layers as a mask The process which etches said tungsten system electric conduction material layer so that the thickness may become the value of zero or its near in a resist non-existence region larger than spacing between said two or more resist layers, By the dry etching which makes etching gas the mixed gas of bromine content gas or iodine content gas, chlorine content gas, and oxygen gas, and uses said two or more resist layers as a mask By removing the tungsten system electric conduction material between said two or more resist layers, controlling side etching of said tungsten system electric conduction material layer with a resultant The dry etching approach including the process which forms two or more tungsten system electric conduction material layers which have a pattern corresponding to said two or more resist layers, respectively.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the approach of carrying out dry etching of the laminating which put W system electric conduction material layers, such as W (tungsten) and WSi2 (tungsten silicide), on the Pori Si (silicon) layer, or the monolayer of W system electric conduction material. By the dry etching which makes etching gas especially the mixed gas of Cl (chlorine) content gas and O2 (oxygen) gas After carrying out just etching of the W system electric conduction material layer, reservation of an anisotropy configuration and mitigation of an etching damage are enabled by adding Br (bromine) content gas or I (iodine) content gas to this mixed gas, and performing over etching.
[0002]
[Description of the Prior Art] Conventionally, as a wiring forming method using the laminating (W polycide layer) which put WSi two-layer on the Pori Si layer, the approach as shown in drawing 11 -13 is learned (for example, refer to JP,7-94469,A).
[0003] WSi [after carrying out deposition formation of the Pori Si layer 3 and WSi two-layer 4 for the front face of a silicon substrate 1 one by one on wrap gate oxide 2 at the process of drawing 11] two-layer -- the resist layers 5a-5d are formed by phot lithography processing on 4. The resist layers 5a and 5b are arranged at big spacing in non-dense pattern space a, and arrange the resist layers 5b-5d at small spacing in dense pattern space b.
[0004] At the process of drawing 12 , just etching is carried out so that thickness may become the value of zero or its near in non-dense pattern space a about the Pori Si layer 3 and the laminating of WSi two-layer 4 by plasma etching which uses F (fluorine) content gas (for example, S2F6 gas). Consequently, WSi two-layer 4a-4d which has a pattern corresponding to the resist layers 5a-5d, respectively remains. Moreover, in dense pattern space b, since an etch rate falls according to the so-called RIElag phenomenon (or micro loading effect), compared with etched section 3e of the Pori Si layer 3 in non-dense pattern space a, 3f of etched sections of the Pori Si layer 3 remains thickly.
[0005] At the process of drawing 13 , plasma etching which uses the mixed gas of Br content gas (for example, HBr gas) and O2 gas performs over etching, and the etched sections in the Pori Si layer 3, such as 3e and 3f, are removed. Plasma etching using the mixed gas of Br system gas, such as HBr, and O2 gas has the high selectivity of the Pori Si layer 3 to gate oxide 2. The Pori Si layers 3a-3d which have a pattern corresponding to the resist layers 5a-5d as a result of over etching, respectively remain. Since the resultant adhering to a pattern side attachment wall controls side etching of WSi two-layer 4a-4d and the Pori Si layers 3a-3d at the time of over etching, an anisotropy configuration can be given to laminatings, such as 4a / 3a and 4b / 3b and 4c / 4d [3c and]/3d. After over etching removes the resist layers 5a-5d. Laminatings, such as 4a/3a, are used as a gate electrode thru/or a wiring layer.
[0006] Conventionally, as a wiring forming method using W layers, the approach as shown in drawing 14 -16 is proposed.
[0007] At the process of drawing 14 , 8 [W-layer] is formed for the front face of the semi-conductor

substrates 6, such as silicon, on the insulator layers 7, such as wrap silicon oxide. And W layers, on 8, the resist layers 9a and 9b are made to approach mutually, and are formed.
[0008] At the process of drawing 15 , just etching is carried out so that W layers of thickness may become the value of zero or its near about 8 by plasma etching which uses SF6 as F content gas in a resist non-existence region larger than spacing between resist layer 9a and 9b. Consequently, while W layer 8a corresponding to the resist layers 9a and 9b and 8b remain, respectively, between 8a and 8b, W layers thin W layer 8c remains according to a RIElag phenomenon.
[0009] It continues at the process of drawing 15 , the same plasma etching as the process of drawing 15 performs over etching, W layer 8c is removed, and W layers 8a and 8b are made to remain at the process of drawing 16 . Then, the resist layers 9a and 9b are removed. W layers 8a and 8b are used as a wiring layer.
[0010] In order to perform anisotropic etching, in drawing 15 and the plasma-etching process by SF6 of 16, it is necessary to make high energy of the ion which carries out incidence to a substrate, or to make temperature of a substrate low. Moreover, the method of controlling side etching with a resultant and securing an anisotropy configuration is also proposed. For example, controlling side etching by WN which is a resultant is shown to JP,7-147271,A by by etching W layers into SF6 with the plasma of the gas which added N2 and NH3. The approach of etching W layers also into JP,10-326774,A with the plasma of the gas which added CHF3 and N2 in SF6 is shown. The bottom of W layers is covered with the film of Ti or Ti compound, and controlling side etching by the titanium fluoride of low vapor pressure generated at the reaction of F and Ti which are etching active species is shown in JP,7-169744,A.
[0011]
[Problem(s) to be Solved by the Invention] According to the approach of drawing 11 -13, it is easy to produce an etching damage on a substrate. That is, at the over etching process of drawing 13 , although the selection ratio of the Pori Si layer 3 to gate oxide 2 is high as mentioned above, since it etches with the plasma of fluorine system gas, the selection ratio of the Pori Si layer 3 to gate oxide 2 is low, and gate oxide 2 may be etched by the just-etching process of drawing 12 . Before the thickness of the Pori Si layer 3 becomes zero, it is necessary to make production control severe, in order to prevent this so that just etching may be stopped. Moreover, since the gate section containing gate dielectric film 2 is exposed to the plasma at the time of just etching of drawing 12 , and the over etching of drawing 13 , it tends to receive the damage by the ion bombardment.
[0012] On the other hand, since it etches with the plasma of fluorine system gas according to the approach of drawing 14 -16, the selection ratio of W to the silicon oxide which constitutes an insulator layer 7 is low, and as shown in drawing 16 , W layers of insulator layers 7 are etched in the side of 8a and 8b in the case of over etching. For this reason, there is un-arranging [to which a wiring level difference becomes large].
[0013] The purpose of this invention is to offer the new dry etching approach which can mitigate an etching damage, securing an anisotropy configuration.
[0014]
[Means for Solving the Problem] The 1st dry etching approach concerning this invention The process which forms the laminating which put the tungsten system electric conduction material layer for the substrate on the polish recon layer on the wrap insulator layer, The process which two or more resist layers are made to approach mutually, and forms them on said tungsten system electric conduction material layer, By the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, and uses said two or more resist layers as a mask The process which etches said tungsten system electric conduction material layer so that the thickness may become the value of zero or its near in a resist non-existence region larger than spacing between said two or more resist layers, By the dry etching which makes etching gas the mixed gas which contains bromine content gas or iodine content gas, and oxygen gas at least, and uses said two or more resist layers as a mask The process which forms two or more tungsten system electric conduction material layers which have a pattern corresponding to said two or more resist layers, respectively by removing the tungsten system electric conduction material

between said two or more resist layers, controlling side etching of said tungsten system electric conduction material layer with a resultant, By the dry etching which makes etching gas the mixed gas of bromine content gas or iodine content gas, chlorine content gas, and oxygen gas, and uses said two or more resist layers and said two or more tungsten system electric conduction material layers as a mask The process which forms two or more polish recon layers which have a pattern corresponding to said two or more resist layers, respectively is included by removing said polish recon layer alternatively.

[0015] According to the 1st dry etching approach, after carrying out just etching of the W system electric conduction material layer of W and WSi2 grade by the dry etching which makes etching gas the mixed gas of the chlorine content gas of Cl2 grade, and O2 gas, bromine content gas (or iodine content gas), such as HBr, is added to this mixed gas, over etching of W system electric conduction material is performed, and dry etching of the Pori Si monolayer is performed after this. In over etching, by setting up the flow rate rate of O2 gas highly, the selection ratio of W system electric conduction material to Pori Si can be made high, and it becomes possible to remove W system electric conduction material alternatively. Moreover, it can etch in over etching, securing an anisotropy configuration about W system electric conduction material by setting the flow rate rate of bromine content gas (or iodine content gas) as a predetermined value. Furthermore, since just etching and over etching are performed in the condition that the Pori Si layer exists on the insulator layer as substrate film, the substrate film (insulator layer) is etched, or they are not exposed to an ion bombardment, and become mitigable [an etching damage].

[0016] The process at which the 2nd etching approach concerning this invention forms a tungsten system electric conduction material layer for a substrate on a wrap insulator layer, The process which two or more resist layers are made to approach mutually, and forms them on said tungsten system electric conduction material layer, By the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, and uses said two or more resist layers as a mask The process which etches said tungsten system electric conduction material layer so that the thickness may become the value of zero or its near in a resist non-existence region larger than spacing between said two or more resist layers, By the dry etching which makes etching gas the mixed gas of bromine content gas or iodine content gas, chlorine content gas, and oxygen gas, and uses said two or more resist layers as a mask By removing the tungsten system electric conduction material between said two or more resist layers, controlling side etching of said tungsten system electric conduction material layer with a resultant The process which forms two or more tungsten system electric conduction material layers which have a pattern corresponding to said two or more resist layers, respectively is included.

[0017] According to the 2nd dry etching approach, after carrying out just etching of the W system electric conduction material layer of W and WSi2 grade by the dry etching which makes etching gas the mixed gas of the chlorine content gas of Cl2 grade, and O2 gas, bromine content gas (or iodine content gas), such as HBr, is added to this mixed gas, and over etching of W system electric conduction material is performed. Also in any of just etching and over etching, since the mixed gas of chlorine content gas and O2 gas is used as etching gas, the selection ratio to the silicon oxide which constitutes the insulator layer as substrate film can improve, and etching of the substrate film (insulator layer) can be controlled. Moreover, in over etching, since side etching of W system electric conduction material is controlled by addition of bromine content gas (or iodine content gas), a good anisotropy configuration can be acquired.

[0018]

[Embodiment of the Invention] Drawing 1 -3 show the wiring forming method concerning 1 operation gestalt of this invention.

[0019] At the process of drawing 1 , the gate dielectric film 12 which consists of silicon oxide by the oxidizing [thermally] method etc. is formed in the front face of the semi-conductor substrates 10, such as silicon. a gate-dielectric-film 12 top -- CVD (chemical vapor deposition) -- deposition formation of the Pori Si layer 14 and WSi two-layer 16 is carried out one by one by law etc. The Pori Si layer 14 and WSi two-layer 16 are for forming a gate electrode thru/or a wiring layer, and the Pori Si layer 14 is formed into low resistance by doping of a conductivity-type decision impurity.

[0020] On WSi two-layer 16, the resist layers 18a-18d are formed according to desired gate electrode and circuit pattern by well-known phot lithography processing. The resist layers 18a and 18b are arranged at big spacing in non-dense pattern space A, and arrange the resist layers 18b-18d at small spacing in dense pattern space B.
[0021] plasma etching which uses the mixed gas (Cl2/O2 gas) of Cl2 gas and O2 gas at the process of drawing 2 -- WSi two-layer -- just etching of 16 is carried out so that thickness may become the value of zero or its near in non-dense pattern space A. Etching at this time was performed using the ECR (electron cyclotron resonance) mold plasma etching system of drawing 4 as an example, and etching conditions were set to pressure:1mTorr microwave power:1000W high-frequency power:50W quantity-of-gas-flow:Cl2/O2=50/10sccm.
[0022] WSi two-layer 16a-16d which has a pattern corresponding to the resist layers 18a-18b as a result of just etching, respectively remains. Moreover, in dense pattern space B, since an etch rate falls according to a RIElag phenomenon, while WSi two-layer 16e and comparatively thin 16f are between WSi two-layer 16b and 16c and WSi two-layer 16c, and 16d, it remains, respectively.
[0023] Then, plasma etching using HBr/Cl2/O2 gas which added HBr gas in Cl2/O2 gas performs over etching, and WSi two-layer 16e and 16f are removed. Etching at this time was performed using the etching system of drawing 4 as an example, and etching conditions were set to pressure:1mTorr microwave power:1000W high-frequency power:50W quantity-of-gas-flow:HBr/Cl2/O2=8.5/21.5/20sccm.
[0024] In over etching, O2 flow-rate rate was made high for making high the selection ratio of WSi2 to Pori Si, and making easy WSi two-layer removal of 16e, 16f, etc. Thus, in Cl2 / O2 etching process that O2 flow-rate rate is high, W is set to WOCl4 with high vapor pressure, a WSi two-layer 16a-16d side attachment wall is etched (side etching), and a WSi two-layer 16a-16d anisotropy configuration is spoiled. So, it etches at the time of over etching, controlling side etching, adding HBr in Cl2/O2 gas, making low WOBr4 and low WBr5 of vapor pressure generate, and forming a protective coat in a WSi two-layer 16a-16d side attachment wall. Consequently, a WSi two-layer 16a-16d anisotropy configuration is secured. Moreover, since just etching and over etching are performed in the condition that the Pori Si layer 14 exists on gate dielectric film 12, gate dielectric film 12 is etched, or it is not exposed to an ion bombardment, and an etching damage is mitigated.
[0025] At the process of drawing 3 , the Pori Si layer 14 is alternatively etched by plasma etching which uses HBr/Cl2/O2 gas by using the resist layers 18a-18d and WSi two-layer 16a-16d as a mask. This etching was performed using the etching system of drawing 4 as an example, and etching conditions were set to pressure:2mTorr microwave power:1000W high-frequency power:35W quantity-of-gas-flow:HBr/Cl2/O2=100/5/5sccm. As other examples of etching conditions, what does not use the chlorine content gas of Cl2 grade is possible, and it can be referred to as microwave power:800-1500W, and quantity-of-gas-flow:HBr/O2=100/5sccm.
[0026] The Pori Si layers 14a-14d which have a pattern corresponding to the resist layers 18a-18d as a result of the selective etching of the Pori Si layer 14, respectively remain. At the time of Pori Si etching, since resultants, such as SiOx and SiBrx, control side etching of WSi two-layer 16a-16d and the Pori Si layers 14a-14d, a good anisotropy configuration can be given to laminatings, such as 16a / 14a and 16b / 14b and 16c / 16d [14c and]/14d. Compared with WSi2, Pori Si has little RIElag and it tends to etch it. After Pori Si etching removes the resist layers 18a-18d by well-known ashing processing. WSi2/Pori Si laminatings, such as 16a/14a, are used as a gate electrode thru/or a wiring layer.
[0027] The artificer conducted various experiments on the high point which can be set up using the etching system of drawing 4 paying attention to the selection ratio of WSi [on etching of WSi2 / Pori Si laminating (W polycide layer), and as opposed to Pori Si in plasma etching which uses Cl2/O2 gas]2.
[0028] The processing room 20 consists of plasma room 22a and reaction chamber 22b in the equipment of drawing 4 . The sample base (electrode) 24 is established in the pars basilaris ossis occipitalis of reaction chamber 22b, and the processed wafer 26 is laid in the top face of the sample base 24.
[0029] RF generator 28 is connected to the sample base 24, for example, the high-frequency power which is 13.56MHz is supplied to it. Reaction chamber 22b is connected to Exhauster VAC while

connecting with the source of gas supply which is not illustrated.
[0030] The 2.45GHz microwave MW is supplied to the upper part of plasma room 22a through the microwave installation aperture 30 from the microwave power source which is not illustrated. An aperture 30 usually consists of quartzes. The solenoid coil 32 is formed so that the upper part of the processing room 20 may be surrounded.
[0031] Etching of WSi2 and Pori Si is performed with the plasma of Cl2/O2 gas using the etching system of drawing 4 , and the result of having investigated O2 flow-rate rate dependency of WSi2 / Pori Si selection ratio is shown in drawing 5 . The 1st sample group containing nine samples which carried out deposition formation of the WSi two-layer through the silicon oxide film on the silicon substrate, and the 2nd sample group containing nine samples which carried out deposition formation of the Pori Si layer through the silicon oxide film on the silicon substrate were used for the experiment. The diameter of each silicon substrate was set to 200mm. It etched by inserting each sample as a processed wafer 26 into the etching system of drawing 4 . Etching conditions were set to pressure:1mTorr microwave power:1400W high-frequency power:50W quantity-of-gas-flow:Cl2+O2=50sccm.
[0032] About nine samples in the 1st sample group, O2 flow-rate rate was changed like 0, 10, 20, 22, 24, 26, 28, and 30 or 40%, and it asked for the etch rate of WSi2 for every sample. Line P shows the result in drawing 5 . Moreover, about nine samples in the 2nd sample group, O2 flow-rate rate was changed like the case of the 1st sample group, and it asked for the etch rate of Pori Si for every sample. Line Q shows the result in drawing 5 .
[0033] WSi2 / Pori Si selection ratio was computed by asking for the ratio of the etch rate of the etch rate / Pori Si of WSi2 for every sample with same O2 flow-rate rate by the 1st sample group and the 2nd sample group. Line R shows the result in drawing 5 .
[0034] If the flow rate rate of O2 is made 30% or more according to the experimental result of drawing 5 , it turns out that it becomes the process conditions into which only WSi2 is etched mostly. In the over etching of drawing 2 , since the flow rate rate of O2 was made into 40%, WSi two-layer which remained to the narrow tooth space, such as 16e and 16f, is efficiently removable. Consequently, the pattern dependency of an etch rate based on the RIElag phenomenon of WSi2 is cancellable.
[0035] Drawing 6 shows the result of having investigated the HBr flow rate rate dependency of the amount of WSi2 side etching in plasma etching which uses HBr/Cl2/O2 gas. Four samples which formed the WSi2/Pori Si laminating (W polycide layer) through the silicon oxide film on the silicon substrate with a diameter of 200mm were used for the experiment. As shown in dense pattern space B of drawing 1 , according to Rhine / tooth-space =1.0 / 0.6-micrometer pattern, many resist layers were installed in each sample side by side. Thus, it etched by inserting each sample which prepared the resist layer as a processed wafer 26 into the etching system of drawing 4 . Etching conditions were set to pressure:1mTorr microwave power:1400W high-frequency power:50W quantity-of-gas-flow:Cl2+HBr=30sccm and O2=20sccm. Here, the O2 flow-rate percentage is 40% which becomes infinite [WSi2 / Pori Si selection ratio] by drawing 1 .
[0036] About four samples, HBr was changed like 0, 10, and 20 or 30% among Cl2+HBr(s), and the amount S of side etching of WSi2 (micrometer) was calculated for every sample. The amount S of side etching can be calculated as width of face Wbot measured on the width-of-face Wtop-base measured by S= top face so that it might illustrate about WSi two-layer 16a to drawing 7 . S< 0 expresses a forward tapered shape configuration, and S> 0 expresses a side etch configuration (back taper configuration), respectively.
[0037] According to the experimental result of drawing 6 , it turns out that side etching serves as zero at 17% of HBr flow rate rates, and a perpendicular anisotropic etching configuration is acquired. However, by Rhine / tooth-space pattern, if it is made the conditions of 17% of HBr flow rate rates, although a perpendicular configuration is acquired, since a lot of resultants adhere to a side attachment wall, it will become a forward tapered shape configuration in isolated Rhine.
[0038] At the process of drawing 2 , since it was made to perform just etching by plasma etching which uses Cl2/O2 gas, generating of the forward tapered shape configuration in isolated Rhine which happened in HBr/Cl2/O2 process can be prevented. Keeping high the selection ratio of WSi2 to Pori Si,

since it was made to perform over etching of WSi2 using HBr/Cl2 / O2 gas plasma-etching process of high O2 flow rate, etching removal only of WSi2 which remained to the narrow tooth space can be carried out, and, moreover, the addition effectiveness of HBr can protect side etching of WSi2.
[0039] Drawing 8 -10 show the wiring forming method concerning other operation gestalten of this invention.
[0040] At the process of drawing 8 , 44 [W-layer] is formed for the front face of the semi-conductor substrates 40, such as silicon, by a spatter etc. on the insulator layers 42, such as wrap silicon oxide. And on 44, according to a desired circuit pattern, the resist layers 46a and 46b are made to approach mutually, and are formed W layers.
[0041] At the process of drawing 9 , just etching is carried out so that W layers of thickness may become the value of zero or its near about 44 by plasma etching which uses Cl2/O2 gas in a resist non-existence region larger than spacing of the resist layers 46a and 46b. Etching at this time can be performed on the same conditions as just etching stated by drawing 2 . While W layer 44a corresponding to the resist layers 46a and 46b and 44b are obtained as a result of just etching, respectively, between 44a and 44b, W layers thin W layer 44c remains according to a RIElag phenomenon.
[0042] Plasma etching using HBr/Cl2/O2 gas which added HBr in Cl2/O2 gas performs over etching, W layer 44c is removed, and W layers 44a and 44b are made to remain at the process of drawing 10 . Etching at this time can be performed on the same conditions as the over etching stated by drawing 2 . After over etching removes the resist layers 46a and 46b by ashing processing etc. W layers 44a and 44b are used as a wiring layer.
[0043] In drawing 9 and etching processing of 10, since Cl2/O2 gas is used as etching gas, the selection ratio of W to the silicon oxide which constitutes an insulator layer 42 improves. Therefore, increase of film decrease of an insulator layer 42 or a wiring level difference can be prevented. Moreover, in the over etching of drawing 10 , since W layers of side etching of 44a and 44b are controlled by addition of HBr, configuration degradation (back taper configuration etc.) of W layers can be prevented.
[0044] As for the wiring forming method described above about drawing 8 -10, the W layers of the operation effectiveness same with having used WSi two-layer, having carried out and having described above are acquired instead of 44.
[0045] This invention is not limited to the above-mentioned operation gestalt, and can be carried out with various alteration gestalten. For example, the following modification is possible.
[0046] (1) As a W system electric conduction material layer, W and not only WSi2 but W alloy may be used. As tungsten silicide, not only a stoichiometry-thing but a nonstoichiometric thing may be used like WSi2, and, generally it is usable in WSix.
[0047] (2) As bromine content gas, not only HBr but Br2, BBr3, CBr4, and SiBr4 grade may be used. What is necessary is just to set up the addition of the gas of Br2 grade so that it may become the case of HBr which the amount of Br atom which exists in the plasma showed with said operation gestalt, and an EQC. Moreover, the iodine content gas of HI, I2, BI3, CI4, and SiI4 grade may be used instead of bromine content gas. About gas, such as HBr or HI, or O2 gas, the optimum value of an addition is that (for example, it is dependent on the membrane formation approach, the processing conditions after membrane formation, membrane formation equipment, etc.) depending on the membraneous quality of the etched film, and adjusting for every etched film is desirable.
[0048] (3) When carrying out dry etching of the W system electric conduction material layer, antireflection films, such as TiN and TiON, may be beforehand prepared on W system electric conduction material layer. Moreover, WN layer etc. may be made to intervene between W system electric conduction material layer and the Pori Si layer.
[0049]
[Effect of the Invention] As mentioned above, since according to this invention bromine content gas (or iodine content gas) is added to this mixed gas, over etching of W system electric conduction material is performed and it was made to perform dry etching of the Pori Si monolayer after this after carrying out just etching of the W system electric conduction material layer by the dry etching which makes etching gas the mixed gas of chlorine-based gas and oxygen gas, an etching damage can be mitigated securing

an anisotropy configuration and the effectiveness that the yield improves is acquired.

[0050] Moreover, since bromine content gas (or iodine content gas) is added to this mixed gas and it was made to perform over etching of W system electric conduction material after carrying out just etching of the W system electric conduction material layer by the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, etching of a substrate insulator layer can be controlled securing an anisotropy configuration, and the effectiveness that the yield improves is acquired.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the approach of carrying out dry etching of the laminating which put W system electric conduction material layers, such as W (tungsten) and WSi2 (tungsten silicide), on the Pori Si (silicon) layer, or the monolayer of W system electric conduction material. By the dry etching which makes etching gas especially the mixed gas of Cl (chlorine) content gas and O2 (oxygen) gas After carrying out just etching of the W system electric conduction material layer, reservation of an anisotropy configuration and mitigation of an etching damage are enabled by adding Br (bromine) content gas or I (iodine) content gas to this mixed gas, and performing over etching.

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PRIOR ART

[Description of the Prior Art] Conventionally, as a wiring forming method using the laminating (W polycide layer) which put WSi two-layer on the Pori Si layer, the approach as shown in drawing 11 -13 is learned (for example, refer to JP,7-94469,A).
[0003] WSi [after carrying out deposition formation of the Pori Si layer 3 and WSi two-layer 4 for the front face of a silicon substrate 1 one by one on wrap gate oxide 2 at the process of drawing 11] two-layer -- the resist layers 5a-5d are formed by phot lithography processing on 4. The resist layers 5a and 5b are arranged at big spacing in non-dense pattern space a, and arrange the resist layers 5b-5d at small spacing in dense pattern space b.
[0004] At the process of drawing 12 , just etching is carried out so that thickness may become the value of zero or its near in non-dense pattern space a about the Pori Si layer 3 and the laminating of WSi two-layer 4 by plasma etching which uses F (fluorine) content gas (for example, S2F6 gas). Consequently, WSi two-layer 4a-4d which has a pattern corresponding to the resist layers 5a-5d, respectively remains. Moreover, in dense pattern space b, since an etch rate falls according to the so-called RIElag phenomenon (or micro loading effect), compared with etched section 3e of the Pori Si layer 3 in non-dense pattern space a, 3f of etched sections of the Pori Si layer 3 remains thickly.
[0005] At the process of drawing 13 , plasma etching which uses the mixed gas of Br content gas (for example, HBr gas) and O2 gas performs over etching, and the etched sections in the Pori Si layer 3, such as 3e and 3f, are removed. Plasma etching using the mixed gas of Br system gas, such as HBr, and O2 gas has the high selectivity of the Pori Si layer 3 to gate oxide 2. The Pori Si layers 3a-3d which have a pattern corresponding to the resist layers 5a-5d as a result of over etching, respectively remain. Since the resultant adhering to a pattern side attachment wall controls side etching of WSi two-layer 4a-4d and the Pori Si layers 3a-3d at the time of over etching, an anisotropy configuration can be given to laminatings, such as 4a / 3a and 4b / 3b and 4c / 4d [3c and]/3d. After over etching removes the resist layers 5a-5d. Laminatings, such as 4a/3a, are used as a gate electrode thru/or a wiring layer.
[0006] Conventionally, as a wiring forming method using W layers, the approach as shown in drawing 14 -16 is proposed.
[0007] At the process of drawing 14 , 8 [W-layer] is formed for the front face of the semi-conductor substrates 6, such as silicon, on the insulator layers 7, such as wrap silicon oxide. And W layers, on 8, the resist layers 9a and 9b are made to approach mutually, and are formed.
[0008] At the process of drawing 15 , just etching is carried out so that W layers of thickness may become the value of zero or its near about 8 by plasma etching which uses SF6 as F content gas in a resist non-existence region larger than spacing between resist layer 9a and 9b. Consequently, while W layer 8a corresponding to the resist layers 9a and 9b and 8b remain, respectively, between 8a and 8b, W layers thin W layer 8c remains according to a RIElag phenomenon.
[0009] It continues at the process of drawing 15 , the same plasma etching as the process of drawing 15 performs over etching, W layer 8c is removed, and W layers 8a and 8b are made to remain at the process of drawing 16 . Then, the resist layers 9a and 9b are removed. W layers 8a and 8b are used as a wiring layer.

[0010] In order to perform anisotropic etching, in drawing 15 and the plasma-etching process by SF6 of 16, it is necessary to make high energy of the ion which carries out incidence to a substrate, or to make temperature of a substrate low. Moreover, the method of controlling side etching with a resultant and securing an anisotropy configuration is also proposed. For example, controlling side etching by WN which is a resultant is shown to JP,7-147271,A by by etching W layers into SF6 with the plasma of the gas which added N2 and NH3. The approach of etching W layers also into JP,10-326774,A with the plasma of the gas which added CHF3 and N2 in SF6 is shown. The bottom of W layers is covered with the film of Ti or Ti compound, and controlling side etching by the titanium fluoride of low vapor pressure generated at the reaction of F and Ti which are etching active species is shown in JP,7-169744,A.

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, since according to this invention bromine content gas (or iodine content gas) is added to this mixed gas, over etching of W system electric conduction material is performed and it was made to perform dry etching of the Pori Si monolayer after this after carrying out just etching of the W system electric conduction material layer by the dry etching which makes etching gas the mixed gas of chlorine-based gas and oxygen gas, an etching damage can be mitigated securing an anisotropy configuration and the effectiveness that the yield improves is acquired.
[0050] Moreover, since bromine content gas (or iodine content gas) is added to this mixed gas and it was made to perform over etching of W system electric conduction material after carrying out just etching of the W system electric conduction material layer by the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, etching of a substrate insulator layer can be controlled securing an anisotropy configuration, and the effectiveness that the yield improves is acquired.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] According to the approach of drawing 11 -13, it is easy to produce an etching damage on a substrate. That is, at the over etching process of drawing 13 , although the selection ratio of the Pori Si layer 3 to gate oxide 2 is high as mentioned above, since it etches with the plasma of fluorine system gas, the selection ratio of the Pori Si layer 3 to gate oxide 2 is low, and gate oxide 2 may be etched by the just-etching process of drawing 12 . Before the thickness of the Pori Si layer 3 becomes zero, it is necessary to make production control severe, in order to prevent this so that just etching may be stopped. Moreover, since the gate section containing gate dielectric film 2 is exposed to the plasma at the time of just etching of drawing 12 , and the over etching of drawing 13 , it tends to receive the damage by the ion bombardment.
[0012] On the other hand, since it etches with the plasma of fluorine system gas according to the approach of drawing 14 -16, the selection ratio of W to the silicon oxide which constitutes an insulator layer 7 is low, and as shown in drawing 16 , W layers of insulator layers 7 are etched in the side of 8a and 8b in the case of over etching. For this reason, there is un-arranging [to which a wiring level difference becomes large].
[0013] The purpose of this invention is to offer the new dry etching approach which can mitigate an etching damage, securing an anisotropy configuration.

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MEANS

[Means for Solving the Problem] The 1st dry etching approach concerning this invention The process which forms the laminating which put the tungsten system electric conduction material layer for the substrate on the polish recon layer on the wrap insulator layer, The process which two or more resist layers are made to approach mutually, and forms them on said tungsten system electric conduction material layer, By the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, and uses said two or more resist layers as a mask The process which etches said tungsten system electric conduction material layer so that the thickness may become the value of zero or its near in a resist non-existence region larger than spacing between said two or more resist layers, By the dry etching which makes etching gas the mixed gas which contains bromine content gas or iodine content gas, and oxygen gas at least, and uses said two or more resist layers as a mask The process which forms two or more tungsten system electric conduction material layers which have a pattern corresponding to said two or more resist layers, respectively by removing the tungsten system electric conduction material between said two or more resist layers, controlling side etching of said tungsten system electric conduction material layer with a resultant, By the dry etching which makes etching gas the mixed gas of bromine content gas or iodine content gas, chlorine content gas, and oxygen gas, and uses said two or more resist layers and said two or more tungsten system electric conduction material layers as a mask The process which forms two or more polish recon layers which have a pattern corresponding to said two or more resist layers, respectively is included by removing said polish recon layer alternatively.
[0015] According to the 1st dry etching approach, after carrying out just etching of the W system electric conduction material layer of W and WSi2 grade by the dry etching which makes etching gas the mixed gas of the chlorine content gas of Cl2 grade, and O2 gas, bromine content gas (or iodine content gas), such as HBr, is added to this mixed gas, over etching of W system electric conduction material is performed, and dry etching of the Pori Si monolayer is performed after this. In over etching, by setting up the flow rate rate of O2 gas highly, the selection ratio of W system electric conduction material to Pori Si can be made high, and it becomes possible to remove W system electric conduction material alternatively. Moreover, it can etch in over etching, securing an anisotropy configuration about W system electric conduction material by setting the flow rate rate of bromine content gas (or iodine content gas) as a predetermined value. Furthermore, since just etching and over etching are performed in the condition that the Pori Si layer exists on the insulator layer as substrate film, the substrate film (insulator layer) is etched, or they are not exposed to an ion bombardment, and become mitigable [an etching damage].
[0016] The process at which the 2nd etching approach concerning this invention forms a tungsten system electric conduction material layer for a substrate on a wrap insulator layer, The process which two or more resist layers are made to approach mutually, and forms them on said tungsten system electric conduction material layer, By the dry etching which makes etching gas the mixed gas of chlorine content gas and oxygen gas, and uses said two or more resist layers as a mask The process which etches said tungsten system electric conduction material layer so that the thickness may become the value of zero or its near in a resist non-existence region larger than spacing between said two or

more resist layers, By the dry etching which makes etching gas the mixed gas of bromine content gas or iodine content gas, chlorine content gas, and oxygen gas, and uses said two or more resist layers as a mask By removing the tungsten system electric conduction material between said two or more resist layers, controlling side etching of said tungsten system electric conduction material layer with a resultant The process which forms two or more tungsten system electric conduction material layers which have a pattern corresponding to said two or more resist layers, respectively is included.
[0017] According to the 2nd dry etching approach, after carrying out just etching of the W system electric conduction material layer of W and WSi2 grade by the dry etching which makes etching gas the mixed gas of the chlorine content gas of Cl2 grade, and O2 gas, bromine content gas (or iodine content gas), such as HBr, is added to this mixed gas, and over etching of W system electric conduction material is performed. Also in any of just etching and over etching, since the mixed gas of chlorine content gas and O2 gas is used as etching gas, the selection ratio to the silicon oxide which constitutes the insulator layer as substrate film can improve, and etching of the substrate film (insulator layer) can be controlled. Moreover, in over etching, since side etching of W system electric conduction material is controlled by addition of bromine content gas (or iodine content gas), a good anisotropy configuration can be acquired.
[0018]
[Embodiment of the Invention] Drawing 1 -3 show the wiring forming method concerning 1 operation gestalt of this invention.
[0019] At the process of drawing 1 , the gate dielectric film 12 which consists of silicon oxide by the oxidizing [thermally] method etc. is formed in the front face of the semi-conductor substrates 10, such as silicon. a gate-dielectric-film 12 top -- CVD (chemical vapor deposition) -- deposition formation of the Pori Si layer 14 and WSi two-layer 16 is carried out one by one by law etc. The Pori Si layer 14 and WSi two-layer 16 are for forming a gate electrode thru/or a wiring layer, and the Pori Si layer 14 is formed into low resistance by doping of a conductivity-type decision impurity.
[0020] On WSi two-layer 16, the resist layers 18a-18d are formed according to desired gate electrode and circuit pattern by well-known phot lithography processing. The resist layers 18a and 18b are arranged at big spacing in non-dense pattern space A, and arrange the resist layers 18b-18d at small spacing in dense pattern space B.
[0021] plasma etching which uses the mixed gas (Cl2/O2 gas) of Cl2 gas and O2 gas at the process of drawing 2 -- WSi two-layer -- just etching of 16 is carried out so that thickness may become the value of zero or its near in non-dense pattern space A. Etching at this time was performed using the ECR (electron cyclotron resonance) mold plasma etching system of drawing 4 as an example, and etching conditions were set to pressure:1mTorr microwave power:1000W high-frequency power:50W quantity-of-gas-flow:Cl2/O2=50/10sccm.
[0022] WSi two-layer 16a-16d which has a pattern corresponding to the resist layers 18a-18b as a result of just etching, respectively remains. Moreover, in dense pattern space B, since an etch rate falls according to a RIElag phenomenon, while WSi two-layer 16e and comparatively thin 16f are between WSi two-layer 16b and 16c and WSi two-layer 16c, and 16d, it remains, respectively.
[0023] Then, plasma etching using HBr/Cl2/O2 gas which added HBr gas in Cl2/O2 gas performs over etching, and WSi two-layer 16e and 16f are removed. Etching at this time was performed using the etching system of drawing 4 as an example, and etching conditions were set to pressure:1mTorr microwave power:1000W high-frequency power:50W quantity-of-gas-flow:HBr/Cl2/O2=8.5/21.5/20sccm.
[0024] In over etching, O2 flow-rate rate was made high for making high the selection ratio of WSi2 to Pori Si, and making easy WSi two-layer removal of 16e, 16f, etc. Thus, in Cl2 / O2 etching process that O2 flow-rate rate is high, W is set to WOCl4 with high vapor pressure, a WSi two-layer 16a-16d side attachment wall is etched (side etching), and a WSi two-layer 16a-16d anisotropy configuration is spoiled. So, it etches at the time of over etching, controlling side etching, adding HBr in Cl2/O2 gas, making low WOBr4 and low WBr5 of vapor pressure generate, and forming a protective coat in a WSi two-layer 16a-16d side attachment wall. Consequently, a WSi two-layer 16a-16d anisotropy

configuration is secured. Moreover, since just etching and over etching are performed in the condition that the Pori Si layer 14 exists on gate dielectric film 12, gate dielectric film 12 is etched, or it is not exposed to an ion bombardment, and an etching damage is mitigated.

[0025] At the process of drawing 3 , the Pori Si layer 14 is alternatively etched by plasma etching which uses HBr/Cl2/O2 gas by using the resist layers 18a-18d and WSi two-layer 16a-16d as a mask. This etching was performed using the etching system of drawing 4 as an example, and etching conditions were set to pressure:2mTorr microwave power:1000W high-frequency power:35W quantity-of-gas-flow:HBr/Cl2/O2=100/5/5sccm. As other examples of etching conditions, what does not use the chlorine content gas of Cl2 grade is possible, and it can be referred to as microwave power:800-1500W, and quantity-of-gas-flow:HBr/O2=100/5sccm.

[0026] The Pori Si layers 14a-14d which have a pattern corresponding to the resist layers 18a-18d as a result of the selective etching of the Pori Si layer 14, respectively remain. At the time of Pori Si etching, since resultants, such as SiOx and SiBrx, control side etching of WSi two-layer 16a-16d and the Pori Si layers 14a-14d, a good anisotropy configuration can be given to laminatings, such as 16a / 14a and 16b / 14b and 16c / 16d [14c and]/14d. Compared with WSi2, Pori Si has little RIElag and it tends to etch it. After Pori Si etching removes the resist layers 18a-18d by well-known ashing processing. WSi2/Pori Si laminatings, such as 16a/14a, are used as a gate electrode thru/or a wiring layer.

[0027] The artificer conducted various experiments on the high point which can be set up using the etching system of drawing 4 paying attention to the selection ratio of WSi [on etching of WSi2 / Pori Si laminating (W polycide layer), and as opposed to Pori Si in plasma etching which uses Cl2/O2 gas]2.

[0028] The processing room 20 consists of plasma room 22a and reaction chamber 22b in the equipment of drawing 4 . The sample base (electrode) 24 is established in the pars basilaris ossis occipitalis of reaction chamber 22b, and the processed wafer 26 is laid in the top face of the sample base 24.

[0029] RF generator 28 is connected to the sample base 24, for example, the high-frequency power which is 13.56MHz is supplied to it. Reaction chamber 22b is connected to Exhauster VAC while connecting with the source of gas supply which is not illustrated.

[0030] The 2.45GHz microwave MW is supplied to the upper part of plasma room 22a through the microwave installation aperture 30 from the microwave power source which is not illustrated. An aperture 30 usually consists of quartzes. The solenoid coil 32 is formed so that the upper part of the processing room 20 may be surrounded.

[0031] Etching of WSi2 and Pori Si is performed with the plasma of Cl2/O2 gas using the etching system of drawing 4 , and the result of having investigated O2 flow-rate rate dependency of WSi2 / Pori Si selection ratio is shown in drawing 5 . The 1st sample group containing nine samples which carried out deposition formation of the WSi two-layer through the silicon oxide film on the silicon substrate, and the 2nd sample group containing nine samples which carried out deposition formation of the Pori Si layer through the silicon oxide film on the silicon substrate were used for the experiment. The diameter of each silicon substrate was set to 200mm. It etched by inserting each sample as a processed wafer 26 into the etching system of drawing 4 . Etching conditions were set to pressure:1mTorr microwave power:1400W high-frequency power:50W quantity-of-gas-flow:Cl2+O2=50sccm.

[0032] About nine samples in the 1st sample group, O2 flow-rate rate was changed like 0, 10, 20, 22, 24, 26, 28, and 30 or 40%, and it asked for the etch rate of WSi2 for every sample. Line P shows the result in drawing 5 . Moreover, about nine samples in the 2nd sample group, O2 flow-rate rate was changed like the case of the 1st sample group, and it asked for the etch rate of Pori Si for every sample. Line Q shows the result in drawing 5 .

[0033] WSi2 / Pori Si selection ratio was computed by asking for the ratio of the etch rate of the etch rate / Pori Si of WSi2 for every sample with same O2 flow-rate rate by the 1st sample group and the 2nd sample group. Line R shows the result in drawing 5 .

[0034] If the flow rate rate of O2 is made 30% or more according to the experimental result of drawing 5 , it turns out that it becomes the process conditions into which only WSi2 is etched mostly. In the over etching of drawing 2 , since the flow rate rate of O2 was made into 40%, WSi two-layer which remained to the narrow tooth space, such as 16e and 16f, is efficiently removable. Consequently, the pattern

dependency of an etch rate based on the RIElag phenomenon of WSi2 is cancellable.
[0035] Drawing 6 shows the result of having investigated the HBr flow rate rate dependency of the amount of WSi2 side etching in plasma etching which uses HBr/Cl2/O2 gas. Four samples which formed the WSi2/Pori Si laminating (W polycide layer) through the silicon oxide film on the silicon substrate with a diameter of 200mm were used for the experiment. As shown in dense pattern space B of drawing 1 , according to Rhine / tooth-space =1.0 / 0.6-micrometer pattern, many resist layers were installed in each sample side by side. Thus, it etched by inserting each sample which prepared the resist layer as a processed wafer 26 into the etching system of drawing 4 . Etching conditions were set to pressure:1mTorr microwave power:1400W high-frequency power:50W quantity-of-gas-flow:Cl2+HBr=30sccm and O2=20sccm. Here, the O2 flow-rate percentage is 40% which becomes infinite [WSi2 / Pori Si selection ratio] by drawing 1 .
[0036] About four samples, HBr was changed like 0, 10, and 20 or 30% among Cl2+HBr(s), and the amount S of side etching of WSi2 (micrometer) was calculated for every sample. The amount S of side etching can be calculated as width of face Wbot measured on the width-of-face Wtop-base measured by S= top face so that it might illustrate about WSi two-layer 16a to drawing 7 . S< 0 expresses a forward tapered shape configuration, and S> 0 expresses a side etch configuration (back taper configuration), respectively.
[0037] According to the experimental result of drawing 6 , it turns out that side etching serves as zero at 17% of HBr flow rate rates, and a perpendicular anisotropic etching configuration is acquired. However, by Rhine / tooth-space pattern, if it is made the conditions of 17% of HBr flow rate rates, although a perpendicular configuration is acquired, since a lot of resultants adhere to a side attachment wall, it will become a forward tapered shape configuration in isolated Rhine.
[0038] At the process of drawing 2 , since it was made to perform just etching by plasma etching which uses Cl2/O2 gas, generating of the forward tapered shape configuration in isolated Rhine which happened in HBr/Cl2/O2 process can be prevented. Keeping high the selection ratio of WSi2 to Pori Si, since it was made to perform over etching of WSi2 using HBr/Cl2 / O2 gas plasma-etching process of high O2 flow rate, etching removal only of WSi2 which remained to the narrow tooth space can be carried out, and, moreover, the addition effectiveness of HBr can protect side etching of WSi2.
[0039] Drawing 8 -10 show the wiring forming method concerning other operation gestalten of this invention.
[0040] At the process of drawing 8 , 44 [W-layer] is formed for the front face of the semi-conductor substrates 40, such as silicon, by a spatter etc. on the insulator layers 42, such as wrap silicon oxide. And on 44, according to a desired circuit pattern, the resist layers 46a and 46b are made to approach mutually, and are formed W layers.
[0041] At the process of drawing 9 , just etching is carried out so that W layers of thickness may become the value of zero or its near about 44 by plasma etching which uses Cl2/O2 gas in a resist non-existence region larger than spacing of the resist layers 46a and 46b. Etching at this time can be performed on the same conditions as just etching stated by drawing 2 . While W layer 44a corresponding to the resist layers 46a and 46b and 44b are obtained as a result of just etching, respectively, between 44a and 44b, W layers thin W layer 44c remains according to a RIElag phenomenon.
[0042] Plasma etching using HBr/Cl2/O2 gas which added HBr in Cl2/O2 gas performs over etching, W layer 44c is removed, and W layers 44a and 44b are made to remain at the process of drawing 10 . Etching at this time can be performed on the same conditions as the over etching stated by drawing 2 . After over etching removes the resist layers 46a and 46b by ashing processing etc. W layers 44a and 44b are used as a wiring layer.
[0043] In drawing 9 and etching processing of 10, since Cl2/O2 gas is used as etching gas, the selection ratio of W to the silicon oxide which constitutes an insulator layer 42 improves. Therefore, increase of film decrease of an insulator layer 42 or a wiring level difference can be prevented. Moreover, in the over etching of drawing 10 , since W layers of side etching of 44a and 44b are controlled by addition of HBr, configuration degradation (back taper configuration etc.) of W layers can be prevented.
[0044] As for the wiring forming method described above about drawing 8 -10, the W layers of the

operation effectiveness same with having used WSi two-layer, having carried out and having described above are acquired instead of 44.

[0045] This invention is not limited to the above-mentioned operation gestalt, and can be carried out with various alteration gestalten. For example, the following modification is possible.

[0046] (1) As a W system electric conduction material layer, W and not only WSi2 but W alloy may be used. As tungsten silicide, not only a stoichiometry-thing but a nonstoichiometric thing may be used like WSi2, and, generally it is usable in WSix.

[0047] (2) As bromine content gas, not only HBr but Br2, BBr3, CBr4, and SiBr4 grade may be used. What is necessary is just to set up the addition of the gas of Br2 grade so that it may become the case of HBr which the amount of Br atom which exists in the plasma showed with said operation gestalt, and an EQC. Moreover, the iodine content gas of HI, I2, BI3, CI4, and SiI4 grade may be used instead of bromine content gas. About gas, such as HBr or HI, or O2 gas, the optimum value of an addition is that (for example, it is dependent on the membrane formation approach, the processing conditions after membrane formation, membrane formation equipment, etc.) depending on the membraneous quality of the etched film, and adjusting for every etched film is desirable.

[0048] (3) When carrying out dry etching of the W system electric conduction material layer, antireflection films, such as TiN and TiON, may be beforehand prepared on W system electric conduction material layer. Moreover, WN layer etc. may be made to intervene between W system electric conduction material layer and the Pori Si layer.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the substrate sectional view showing the resist layer formation process in the wiring forming method concerning 1 operation gestalt of this invention.
[Drawing 2] It is the substrate sectional view showing WSi two-layer the just-etching process and over etching process following the process of drawing 1 .
[Drawing 3] It is the substrate sectional view showing the Pori Si layer etching process and resist layer removal process following the process of drawing 2 .
[Drawing 4] It is the sectional view showing the plasma etching system used for implementation of this invention.
[Drawing 5] It is the graph which shows O2 flow-rate rate dependency of the selection ratio (WSi2/Pori Si) in plasma etching using Cl2/O2 gas.
[Drawing 6] It is the graph which shows the HBr flow rate rate dependency of the amount of WSi2 side etching in plasma etching using HBr/Cl2/O2 gas.
[Drawing 7] It is the sectional view showing the WSi two-layer side etching situation in WSi2/Pori Si laminating etching.
[Drawing 8] It is the substrate sectional view showing the resist layer formation process in the wiring forming method concerning other operation gestalten of this invention.
[Drawing 9] It is the substrate sectional view showing the just-etching process of W layers following the process of drawing 8 .
[Drawing 10] It is the substrate sectional view showing the over etching process following the process of drawing 9 .
[Drawing 11] It is the substrate sectional view showing the resist layer formation process in an example of the conventional wiring forming method.
[Drawing 12] It is the substrate sectional view showing the just-etching process of WSi2 / Pori Si laminating following the process of drawing 11 .
[Drawing 13] It is the substrate sectional view showing the over etching process and resist layer removal process following the process of drawing 12 .
[Drawing 14] It is the substrate sectional view showing the resist layer formation process in other examples of the conventional wiring forming method.
[Drawing 15] It is the substrate sectional view showing the just-etching process of W layers following the process of drawing 14 .
[Drawing 16] It is the substrate sectional view showing the over etching process following the process of drawing 15 .
[Description of Notations]
10, 40:semi-conductor substrate, 12, 42:insulator layer, 14, the Pori Si layer, 16:WSi two-layer, 18a-18d, 46a, 46b: A resist layer, 44:W layers.

[Translation done.]

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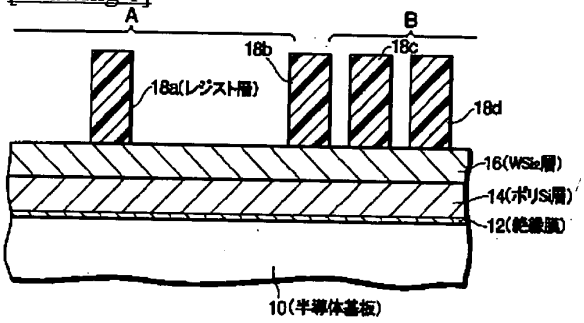
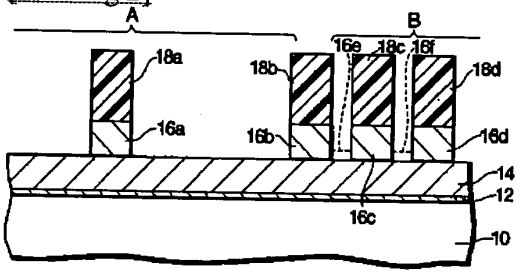
DRAWINGS

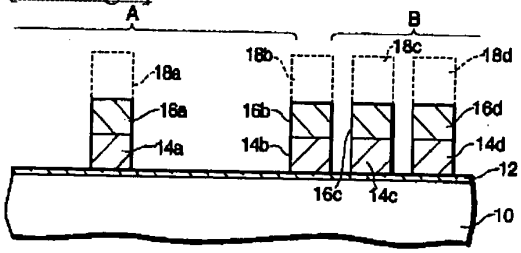
[Drawing 1]



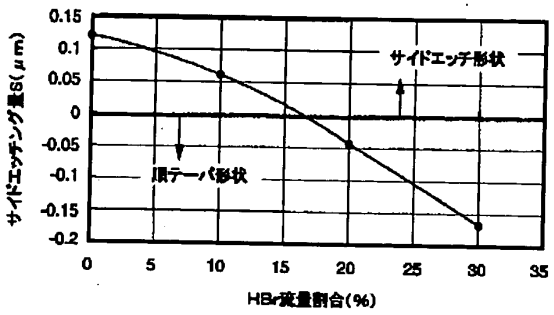
[Drawing 2]



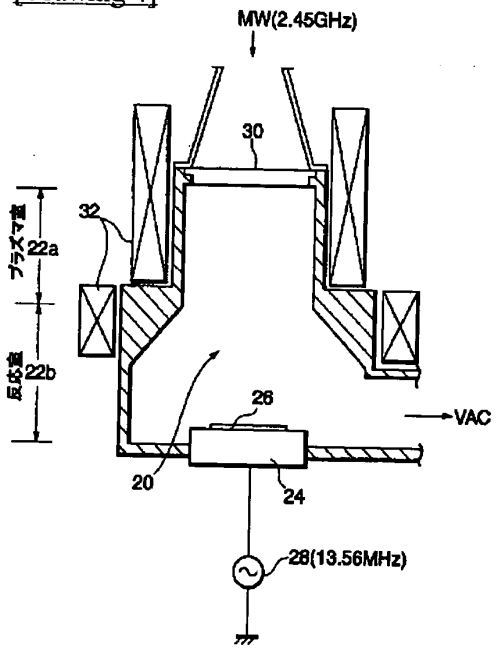
[Drawing 3]



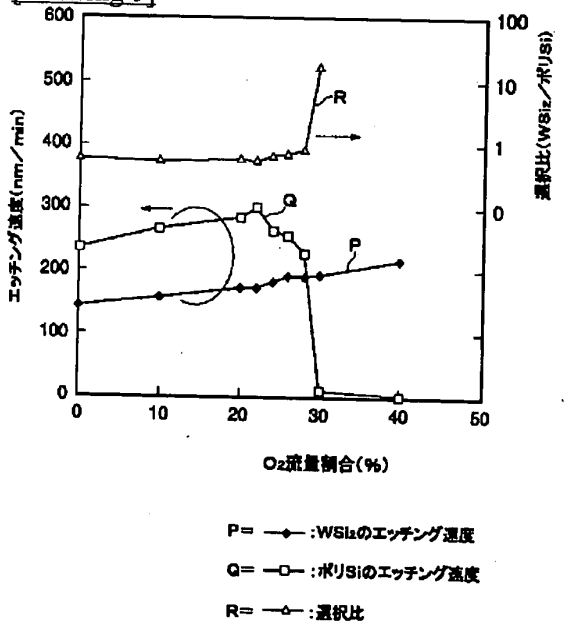
[Drawing 6]



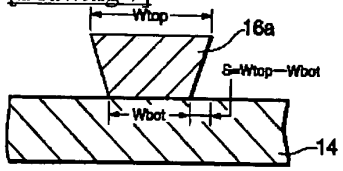
[Drawing 4]



[Drawing 5]



[Drawing 7]



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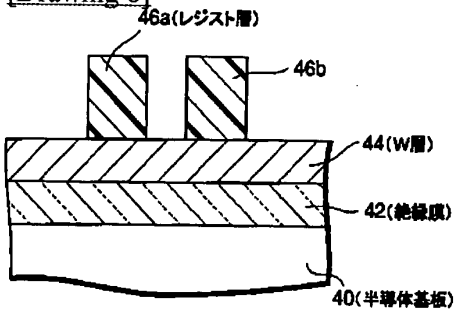
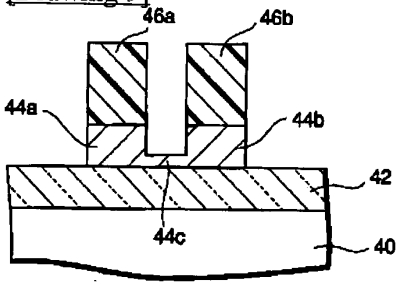
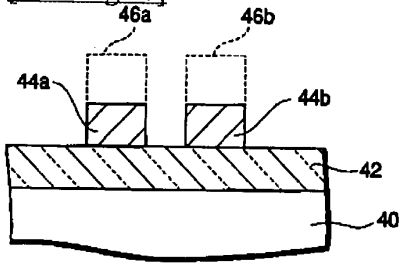


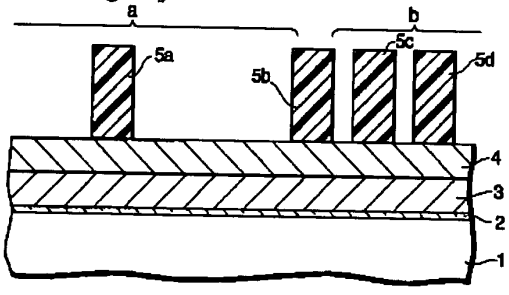
[Drawing 9]



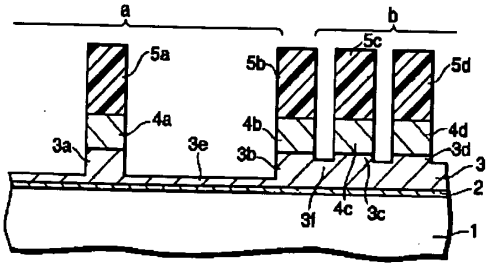
[Drawing 10]



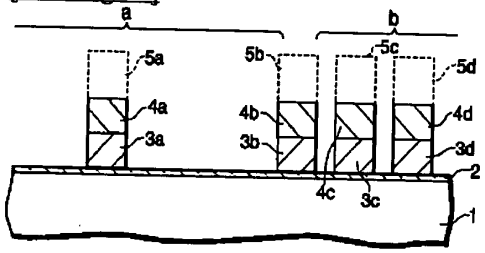
[Drawing 11]



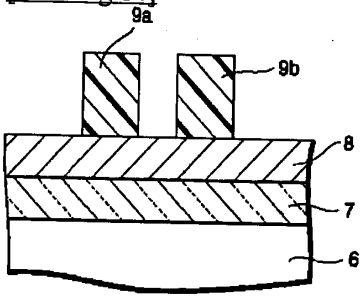
[Drawing 12]



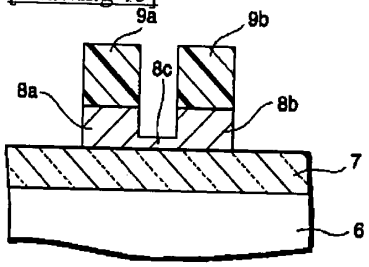
[Drawing 13]



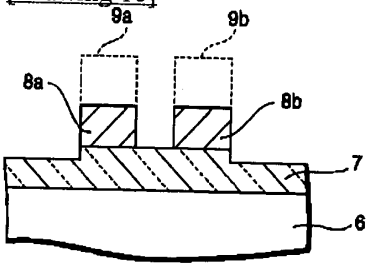
[Drawing 14]



[Drawing 15]



[Drawing 16]



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